CLAIMS

What is claimed is:

1. A microwave/millimeter-wave monolithic integrated circuit device, comprising:

a semiconductor substrate;

at least one first mesa portion and at least one second mesa portion, the first and second mesa portions being formed on the substrate;

at least one PIN diode, the PIN diode being formed on the first mesa portion and including a PIN anode region;

at least one Schottky diode, the Schottky diode being formed on the second mesa portion and including a Schottky anode region; and

a passivation layer deposited on the substrate to cover the PIN diode, the Schottky diode, the first mesa portion, and the second mesa portion while providing access to at least the PIN anode region and the Schottky anode region,

wherein the PIN anode region is formed in approximately the same plane as the Schottky anode region.

2. The microwave/millimeter-wave monolithic integrated circuit device of claim 1 wherein the semiconductor substrate comprises a silicon substrate.

ATTORNEY DOCKET NO. TYCO-017XX
WEINGARTEN, SCHURGIN,
GAGNEBIN & HAYES LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

3. The microwave/millimeter-wave monolithic integrated circuit device of claim 1 wherein the passivation layer comprises a low-loss glass passivation layer.

4. The microwave/millimeter-wave monolithic integrated circuit device of claim 1 wherein the Schottky anode region is formed subsequent to the deposition of the passivation layer.

5. The microwave/millimeter-wave monolithic integrated circuit device of claim 1 wherein the Schottky anode region includes a thin epitaxial layer formed by an ultra-high vacuum chemical vapor deposition process.

6. The microwave/millimeter-wave monolithic integrated circuit device of claim 5 wherein the thin epitaxial layer of the Schottky anode region has a thickness equal to about 0.1 μm.

7. The microwave/millimeter-wave monolithic integrated circuit device of claim 1 wherein the first and second mesa portions are formed on the substrate by way of a single anisotropic etching operation.

8. A method of fabricating a microwave/millimeter-wave monolithic integrated circuit device including at least one PIN diode and at least one Schottky diode, comprising the steps of:

providing a semiconductor substrate;

ATTORNEY DOCKET NO. TYCO-017XX
WEINGARTEN, SCHURGIN,
GAGNEBIN & HAYES LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

forming at least one first mesa portion and at least one second mesa portion on the substrate;

forming the PIN diode including a PIN anode in a PIN diode region of the substrate, the PIN diode being formed on the first mesa portion;

forming the Schottky diode including a Schottky anode in a Schottky diode region of the substrate, the Schottky diode being formed on the second mesa portion, the Schottky anode being formed in approximately the same plane as the PIN anode; and

depositing a passivation layer on the substrate to cover the PIN diode, the Schottky diode, the first mesa portion, and the second mesa portion while providing access to at least the PIN anode and the Schottky anode.

9. The method of claim 8 wherein the providing step includes providing a silicon substrate.

10. The method of claim 8 wherein the depositing step includes depositing a low-loss glass passivation layer on the substrate.

11. The method of claim 8 wherein the first forming step includes forming the first mesa portion and the second mesa portion on the substrate by way of a single anisotropic etching operation.

12. The method of claim 11 wherein the first forming step includes depositing a layer of silicon nitride on

ATTORNEY DOCKET NO. TYCO-017XX
WEINGARTEN, SCHURGIN,
GAGNEBIN & HAYES LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

the PIN diode region and the Schottky diode region of the substrate, masking portions of the PIN diode region and the Schottky diode region that are to become the first and second mesa portions, etching the silicon nitride layer except in the masked portions of the PIN diode and Schottky diode regions, and conducting the single anisotropic etching operation to form the first and second mesa portions on the substrate.

13. The method of claim 8 wherein the second forming step includes etching an implant window for the PIN anode in the PIN diode region of the substrate while masking the Schottky diode region of the substrate, and implanting a dopant through the implant window for the PIN anode in the PIN diode region of the substrate while masking the Schottky diode region of the substrate.

14. The method of claim 8 wherein the third forming step includes forming the Schottky anode subsequent to the deposition of the passivation layer.

15. The method of claim 14 wherein the third forming step includes forming a thin epitaxial layer of the Schottky anode in the Schottky diode region of the substrate by an ultra-high vacuum chemical vapor deposition process while masking the PIN diode region of the substrate.

ATTORNEY DOCKET NO. TYCO-017XX
WEINGARTEN, SCHURGIN,
GAGNEBIN & HAYES LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

16. The method of claim 15 wherein the third forming step includes forming the thin epitaxial layer of the Schottky anode at a predetermined temperature less than a transition temperature of the passivation layer.

ATTORNEY DOCKET NO. TYCO-017XX
WEINGARTEN, SCHURGIN,
GAGNEBIN & HAYES LLP
TEL. (617) 542-2290
FAX. (617) 451-0313